

Features

General

- High-performance, Low-power secure AVR[®] RISC Architecture
- 137 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low Power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to $\pm 6000V$
- Operating Ranges: 2.7V to 5.5V
- Compliant with GSM, 3GPP and EMV 2000 Specifications; PC Industry Compatible
- Available in Wafers, Modules, and Industry-standard Packages

Memory

- 144K Bytes of FLASH Program Memory
- 144K Bytes of EEPROM, Including 128 OTP Bytes and 384-byte Bit-addressable Area
 - 1 to 128-byte Program / Erase
 - 1.25 ms Program / 1.25 ms Erase
 - Typically More than 500,000 Write/Erase Cycles at a Temperature of 25°C
 - 10 Years Data Retention
 - EEPROM Erase Only Mode
 - Write EEPROM With or Without Autoerase
- 8K Bytes of RAM
- 32K Bytes of ROM Dedicated to Atmel's Crypto-library

Peripherals

- Two I/O Ports
 - Configurable to Support Communication Protocols, Including ISO7816-3 and 2-wire protocols
- ISO7816 Controller
 - Up to 625 kbps at 5 MHz
 - Compliant with T=0 and T=1 Protocols
- Serial Peripheral Interface (SPI) Controller (up to 12 MHz)
- Programmable Internal Oscillator
 - Up to 10 MHz on FLASH
 - Up to 40 MHz for Cryptographic Accelerator
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level, 8-vector Interrupt Controller
- 32-bit Cryptographic Accelerator for Public Key Operations Including
 - RSA, DSA, ECC, Diffie-Hellman
- Hardware DES and Triple DES (DPA Resistant)
- Checksum Accelerator
- CRC 16 and 32 Engine (Compliant with ISO/IEC 3309)

Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Light Protection
- Temperature Monitor
- Secure Memory Management/Access Protection (Supervisor Mode)



Secure Microcontroller for Smart Cards

AT90SC 144144CT Summary

6521BS-SCIC-20Dec06



Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

Development Tools

- Voyager Emulation Platform (ATV4 Standard) to Support Software Development
- IAR Embedded Workbench® V3.20c Debugger or Atmel's AVR Studio® Version 4.07 or Above
- Software Libraries and Application Notes

Certification

- EAL4+
- VISA
- CAST
- FIPS

Description

The AT90SC144144CT is a low-power, high-performance, 8/16-bit microcontroller with ROM program memory, EEPROM data memory, based on the secureAVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90SC144144CT achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

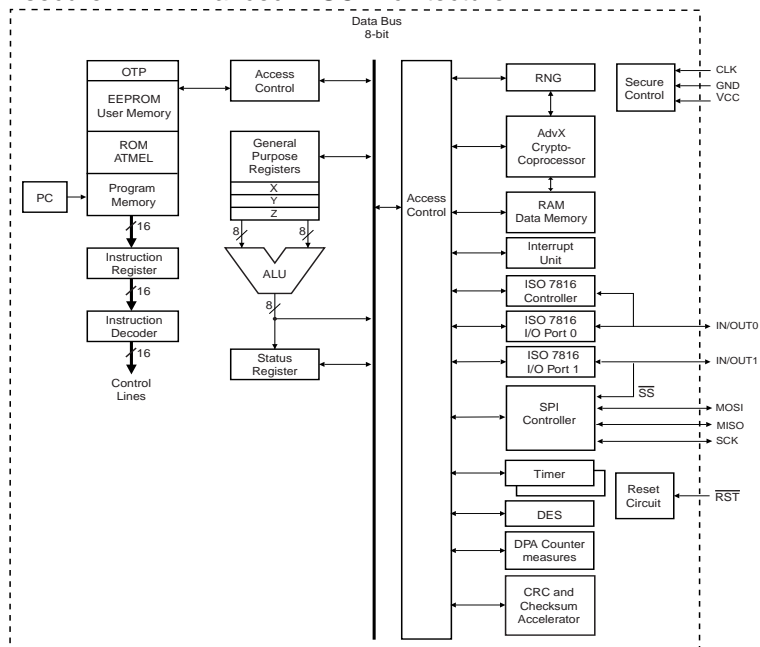
The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versatile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many smart card applications. The AT90SC144144CT benefits of advanced EEPROM functions (XP Mode), but can also be configured to offer compatibility with previous product generations (e.g. AT90SC25672R or AT90SC19236R).

The cryptographic accelerator, running with the secureAVR core, featured in the AT90SC144144CT series is the new AdvX⁹⁶⁰. It is based on a 32-bit multiplier-accumulator architecture which is designed to perform fast encryption and authentication functions. This enables fast computation and low-power operation. The controlling firmware is located either in the dedicated ROM memory (Atmel's cryptolibrary supports standard finite field arithmetic functions including RSA, DSA, DH and ECC) or in the ROM program memory (customer specific).

Additional security features include power and frequency protection logic, logical scrambling on program data and addresses, Power Analysis countermeasures and memory accesses controlled by a supervisor mode.

Figure 1 shows the AT90SC144144CT block diagram.

Figure 1. AT90SC144144CT secureAVR Enhanced RISC Architecture





Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests

www.atmel.com/literature

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Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

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44306 Nantes Cedex 3, France
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13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
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